The Evolution of the Jet Propulsion Laboratory/NASA Iris Deep-Space Transponder

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ABSTRACT

In 2013, the Jet Propulsion Laboratory (JPL) developed the Iris Deep Space transponder, a CubeSat compatible software-defined radio (SDR), intended to support of the first CubeSat deep space mission: the Interplanetary NanoSpacecraft Pathfinder In Relevant Environment (INSPIRE). The Iris Transponder is a reconfigurable SDR designed for missions requiring interoperability with NASA's Deep Space Network (DSN) on X-band frequencies (7.2 GHz uplink, 8.4 GHz downlink). The transponder provides radiometric tracking support with the DSN to provide navigational products for precise orbit determination while performing standard uplink and downlink communications in a CubeSat/SmallSat-applicable package size. In 2015, JPL developed the second version of the Iris Deep-Space Transponder to be used on the Mars Cube One (MarCO) mission. The second version has in addition to X-Band transmit and receive functionality, the capability to receive in the UHF band. For MarCO, Iris successfully performed bent-pipe relay direct-to-Earth during entry, descent, and landing (EDL) of the InSight lander, providing the first confirmation of successful landing, including InSight's first image from the surface of Mars. Currently, a third version of Iris is being developed to be used on secondary payload missions of the upcoming Artemis 1 (previously known as Space Launch System Exploration Mission One (SLS EM-1)). In this version, several updates were made. The power supply board (PSB) was redesigned to increase the radiation tolerance, and further miniaturization was performed to reduce the overall SwaP (Size, Weight, and Power) of the unit. Also, two enhanced navigation and ranging techniques are in development. Namely, the Pseudo-random Noise (PN) Delta Differential One-way Ranging (DDOR) technique as well as PN Regenerative Ranging. This presentation/paper discusses the evolution of the Iris transponder and provides a summary of the key design aspects and specifications.

INTRODUCTION

A deep space transponder is a radio system that transmits and receives simultaneously on diverse frequencies in support of coherent Doppler and range measurements, spacecraft commanding, and telemetry return. A highly stable signal is uplinked from Earth to the transponder which phase locks its downlink carrier to an integer ratio of the received uplink. The downlink is then received on the same Earth station and measured against the uplink reference (two-way Doppler scenario) or at a different Earth station (three-way Doppler scenario) against a coordinated time and frequency reference to produce high precision Doppler signatures for navigation processing. The turnaround signal can also support modulated ranging signals, typically tones (sine waves) or pseudo-noise (PN) sequences to determine absolute range to the spacecraft. The uplink also carries commands from Earth to the spacecraft and the downlink carries telemetry, including science and housekeeping data, from the spacecraft to Earth.

The Jet Propulsion Laboratory (JPL) provides equipment and operational services for both ends of the deep space link, in the form of flight transponders and Deep Space Network (DSN) ground station transmitters and receivers. For the flight transponders JPL has developed first the Small Deep Space Transponder (SDST) which is ASIC-based, and then developed reconfigurable transponders such as the Electra Proximity Operations UHF transceiver [1] which is responsible for most of the data returned from the Mars Science Laboratory via Mars orbiting relays. More recently, JPL developed the Universal Space Transponder (UST) that can support both the deep space and relay links simultaneously [2]. The newest entry in this product line is the Iris CubeSat Compatible, DSN compatible deep space transponder. JPL developed the Iris transponder with the necessary navigational products and basic telecom functions to enable CubeSat science missions to lunar and deep space destinations. The first-generation Iris was designed for the Interplanetary NanoSpacecraft Pathfinder In Relevant Environment (INSPIRE) mission [3]. The modular SDR design of Iris allowed rapid synergistic development parallel to other JPL radio products, and the transponder was further developed and matured for the Mars Cube One (MarCO) mission to Mars [4]. Currently, an updated version of Iris is being built to support seven

out of the thirteen CubeSat mission that are planned to fly as secondary payloads on the Artemis 1. These deep-space CubeSats have a variety of unique scientific pursuits, ranging from mapping the presence of water on the moon to investigating space-radiation effects on the biology of yeast to flying by and return data from an asteroid representative of Near-Earth Asteroids (NEAs) that may one day be human destinations [5].
This paper provides a description of the evolution of the Iris transponder and give a brief description of the different generations of Iris and the key improvements that were made with each generation. For more detailed description of the different Iris versions, please see [3 and 5]. Figure 1 shows the three iterations of Iris. Iris consumes less than 1 U of volume, 1 kg mass, and features a significant subset of standard deep space transponder features, largely inherited from UST and Electra in the form of complex digital signal processing code hosted in Field Programmable Gate Array (FPGA). Iris also shares the basic hardware architecture with these larger transponders but in a more compact form. The main limitation of Iris compared to its larger siblings is not data formats and measurement precision, which are similar, but the smaller amount of power consumed from the spacecraft bus and radiated on the downlink. Iris is a highly capable transponder that is compatible with the DSN in the same sense that all deep space transponders in use today are [3].

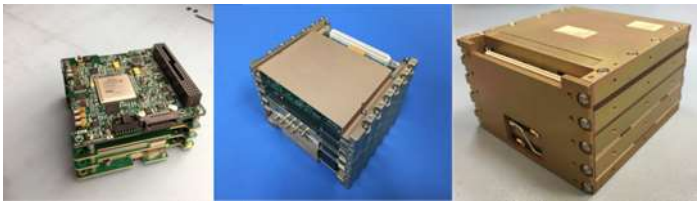

Fig. 1. Iris V.1 (INSPIRE), V2 (MarCO) and V2.1 (Artemis-1) Transponders

IRIS V1.0 (INSPIRE VERSION)

Iris V1.0 Architecture

Iris V.1 is a stacked set of four CubeSat-size boards interconnected, as seen in Fig. 2, with a Pumpkin standard PC-104 connector [6]. The spacecraft interface is Serial Peripheral Interface (SPI), also interconnected via the PC-104. Iris VI is assembled entirely from commercial off the shelf (COTS) parts, but the parts and architecture used have radiation hardened equivalents so that a more environmentally robust (and more expensive) model was produced for the subsequent versions (MarCOs and Artemis -1). The INSPIRE approach to radiation events is to conduct a 90-days mission and to tolerate radiation induced upsets through power-cycle resets as needed.

On top of the Iris stack is the Marina-2 FPGA board featuring a commercial grade Virtex 5, bus power conversion for digital electronics, and associated circuitry. Digital modem signal processing and data handling are performed here. The power supply board (PSB) is below the digital FPGA board and its function is to convert spacecraft bus voltage (nominal 7.4-8.3 VDC for a 3U CubeSat such as INSPIRE) to the voltages required by the receiver and exciter boards. These are separate from the digital power rails on the Marina-2 board for noise control reasons. When powering Iris up, the Marina-2 board is powered first and the other boards are activated under its control. All power converters are designed to limit inrush to a CubeSat bus acceptable level of 3 Amperes peak. The receiver board, below the PSB, performs a single conversion of X-Band radio frequency (RF) at 7.2 GHz to a 112.5 MHz intermediate frequency (IF). The local oscillator (LO) for this down-conversion is provided by a phase locked loop (PLL) whose frequency is set under FPGA control. The IF is sub-harmonic sampled in quadrature and digitized at 12.5 Msps. These samples are then passed to the FPGA for baseband processing. The receiver has a demonstrated carrier acquisition sensitivity of better than -130 dBm and an RF passband suitable for use in any channel of the near Earth or deep space X-Band uplink allocations, that is, 7.14 - 7.24 GHz [3]. The front-end noise figure is approximately 5 dB and the IF bandwidth is 15 MHz. Covers are used on the receiver board to provide RF isolation from other nearby electronics and to provide a thermal heat removal path. At the bottom of the stack is the exciter (or "transmitter") board which generates a carrier frequency using a PLL under FPGA control that is about 2 MHz away from the intended transmission channel. This carrier is then quadrature modulated with baseband samples produced in the signal processing firmware of the FPGA to produce carrier, subcarrier, modulation as required for the mode selected, and shifting to the assigned carrier channel. A balanced vector modulator is used to suppress the original carrier frequency and images, 2 MHz and 4 MHz away from the intended signals respectively, to acceptable levels. The exciter board also hosts the 50 MHz Temperature Compensated Crystal Oscillator (TCXO) that provides the reference frequency for all onboard operations: transmit and receive PLLs, digital to analog (DAC) and analog to digital (ADC) conversion, and FPGA clocking. All digital processing operations are therefore coherent to this oscillator. A metal cover is used on the exciter board to provide RF isolation to other nearby electronics and to provide a heat sink for the board, particularly the power amplifier (PA) parts that dissipate approximately 3 Watts of heat when operating. The PA used in this version of lris is a solid state power amplifier capable of 1 W (30 dBm) RF output but, for the INSPIRE mission, was biased to approximately 0.2 W (23 dBm) so as to reduce overall DC power draw.

Power is supplied to Iris at a nominal 7.4 VDC from the spacecraft power system. Iris consumes 12.75 W in full transponder operation, 6.4 W receive only, and 2.6 W when operating only the Marina-2 board. Figure 2 shows the four-stacked boards of Iris V.1.0. For more detailed description of Iris V1.0 and tests and verification results, see [3].

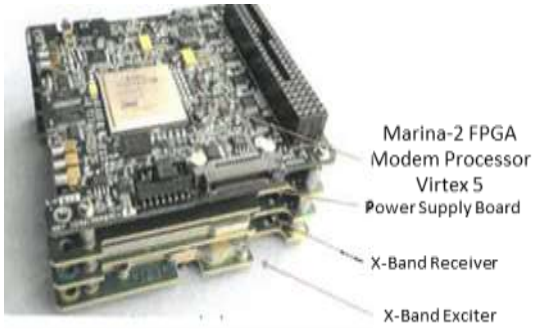

Fig. 2. Iris V.1 Assembled Flight Transponder Stack

Iris V1.0 Firmware and Modem Signal Processing Description

Large portions of the Modem Processor signal-processing chain are heritage design from the Electra product line of JPL SDRs. This synergistic development has proven extremely valuable to all JPL radio product lines where improvements from one product can be directly incorporated to other JPL SDRs [5]. All of the modulation schemes are implemented as baseband signal processing in the Virtex 5 FPGA, including the correct carrier frequency shift of the downlink carrier to match the uplink carrier frequency at the 880/749 turnaround ratio, to within a few microHertz. Only two frequencies are generated by PLL onboard, the receive down-conversion frequency and the transmit frequency. After down conversion, the FPGA operates on the uplink signal at a baseband frequency of several MHz, detecting and locking on the carrier, measuring its phase to feed frequency adjustments into the downlink frequency and phase generation algorithm, detecting and removing the subcarrier, and finally detecting, decoding and sequentially buffering uplink bits. The signal processing involved provides internal, digital automatic gain control (AGC) to several of these demodulation stages and also provides an analog AGC output signal in the form of a variable width pulse train that is smoothed in an op-amp integrator and applied to analog RF gain stages.

Similarly, all of the carrier and subcarrier modulations described above are performed on the downlink signal at a baseband frequency of about 2 MHz (as adjusted for coherence with uplink) and are provided as modulation to the PLL generated downlink carrier about 2 MHz away from the intended frequency. All of these signal processing manipulations result in a stream of "I and Q" ("inphase" and "quadrature") signals that proceed to the X-Band vector modulator.

The 50 MHz TCXO used on Iris Vl.0 (inexpensive COTS) doesn't have the phase stability that is sufficient for 1-way radio metric measurements but is sufficient for telecom. This is mitigated by several factors. First, the absolute frequency of the non-coherent downlink (that is, before a DSN uplink is present) is unimportant as long as it is within the 200 KHz search window of the ground receiver. The drift of the crystal is unimportant as long as it is sufficiently slow, comparable to Doppler signatures. The close-in stochastic phase noise, however, is problematic in terms of downlink acquisition at the high performance and narrow bandwidth DSN receivers. Fortunately, this close in phase noise is minimal when the temperature is very stable, as it is the case when operating in the vacuum of space. It is also possible to adjust the DSN receiver parameters to accommodate a noisier non-coherent downlink signal if necessary, at some cost in SNR. Once Iris is acquired by the DSN and coherence with an uplink is established, the uplink signal is extremely stable (modified only by media effects and Doppler) and the signal processing in FPGA easily tracks out local reference oscillator frequency drift, substantially removing them from the downlink [3]. It is worth emphasizing that the tracking loops don't help with mitigating the phase noise.

For low data rates typically encountered in deep-space applications, the uplink data needs to be modulated on a subcarrier to prevent data power from falling within the carrier recovery loop bandwidth. The uplink to Iris is 1000 bits per second NRZ modulated onto a 16 KHz sinewave subcarrier modulated on the uplink carrier. Receive frames are buffered on Iris and sent to C&DH for de-framing. Other uplink rates are supported by Iris modems, but only the 1000 bps is used and tested for INSPIRE [3]. Downlinks from Iris are supported at multiple rates. 62.5, 250, 1000, and 4000 bps are BPSK modulated onto a 25 KHz subcarrier. Rates of 16000 and 64000 bps are modulated onto a 281.25 MHz subcarrier, and 260,416 bps is modulated directly onto the X-Band carrier. (The two highest rates are slightly non-standard. This was corrected in future versions of Iris.) Downlink frames are convolutional encoded (r=l/2, k=7) meaning that the modulated symbol rate is twice the bit rate. When using the highest rate, for example, 520,832 symbols per second are modulated onto the carrier.

Iris V1.0 C&DH Interface and Concept of Operations

Iris V1.0 does not feature a sequential processor although a CPU was used in subsequent Iris versions. The FPGA interacts directly via SPI with the spacecraft Command and Data Handling (C&DH) processor which reads and writes appropriate command values to FPGA registers. The Multi-Mission Telecommunication Interface module, or MTIF for short, performs the data-handling functions for uplink and downlink. MTIF is the standard interface controller used on Command and Data Handling (C&DH) subsystems for JPL missions such as the Mars Science Laboratory and Soil Moisture Active Passive missions. It is capable of uplink command decoding, error checking, rate selection, and encoding downlink data using various forward-error correction algorithms including Reed-Solomon and Turbo codes Convolutional encoding, on the other hand, is done by the Modem. On Iris, decoded uplink commands are pushed into the uplinked buffer for collection by the C&DH and is primarily handled outside the context of the software for simplicity. Downlink data on the other hand includes software processing, done by C&DH for V1.0, to form standardized frames prior passing them to MTIF for encoding.

Uplink and downlink buffers are double, ping pong style. Spacecraft science and telemetry data are written by C&DH into downlink MTIF buffers from which they are clocked into the FPGA modems for downlink to Earth. Commands received via FPGA modems from the uplink are buffered into MTIF uplink buffers and read by C&DH. MTIF supports a special "FireCode" command that causes the FPGA to latch a spacecraft reset line that cycles power on the entire spacecraft. From the spacecraft C&DH point of view, Iris is the Marina-2 FPGA board on the SPI bus. When Iris is first powered, only the Marina-2 board is active. Receiver and exciter boards can then be activated by command values written into FPGA interface registers. The nominal sequence of events when interacting with the Deep Space Network (DSN) is for Iris to begin a pass by transmitting, on the Earth direction antenna, an unmodulated carrier at its "Best Lock Frequency" (BLF) which is nominally at its assigned X-Band channel. The DSN station (DSS) points at the predicted spacecraft location in the sky and listens on the predicted Doppler corrected frequency. An uplink carrier is then initiated and swept across what is expected to be the Doppler corrected spacecraft receive frequency. When this carrier is detected at the spacecraft, the receiver locks on it and the downlink frequency then locks, by means of signal processing in the FPGA, to exactly 880 / 749 times the uplink frequency. This causes the downlink to jump from BLF to the new "coherent" downlink frequency and so it must be reacquired in the DSN receiver. Once these steps are complete, navigation measurements and two-way data transfer commence.

Iris V1.0 Doppler and Ranging Navigation Features

The uplink carrier frequency is precisely referenced to a maser clock at the DSN station. The downlink carrier is phase locked to the received uplink carrier and thus also phase locked to the very precise ground based MASER reference. This is a measure of how fast the DSN station and spacecraft are moving with respect to each other and can be measured with a precision equivalent to a fraction of a millimeter per second [3]. In processing this data, navigators compare the measured carrier phase to the "predicted" or "model" carrier phase and use this information to correct the assumed state vector of the spacecraft. Doppler data is most useful when there is a measurable change in the value such as is experienced when a spacecraft is in orbit about or passing near Earth, moon, or a planet. The Doppler signature from INSPIRE as it drifts slowly away from Earth was expected to be comparatively benign. During a tracking session, it is possible to make an absolute range measurement of distance from the DSN station to the spacecraft. The station modulates a series of sinusoidal ranging tones onto the uplink carrier. This modulation is detected at baseband in Iris and re-modulated onto the downlink non-regeneratively. The highest frequency ranging tone used is about 1 MHz and has a wavelength of about 300 meters. Other tones at longer wavelengths are used in sequence, the returned phase of each being measured precisely on Earth. The resulting collection of phase measurements is then used to find the absolute distance to the spacecraft with an ambiguity of several tens of kilometers. As the predicted position of the spacecraft is typically within several tens of kilometers of correct, this data is adequate to refine range knowledge to around a meter.

IRIS V2.0 (MARCO VERSION)

The version of Iris that was developed for the two MarCO spacecraft was the basis for the version that is being developed for the Artemis-1 mission except for the additional UHF receive slice. Therefore, in this section, we will focus on describing the UHF receive slice and leave the discussion of the other features for the next section. Traditionally, two separate telecom systems with two separate radios are used to meet the two requirements of having a direct-to-Earth (DTE) communications link with the Deep Space Network (DSN) ground stations, and bent-pipe (BP) relay communications link from InSight through MarCO to the DSN during the entry, descent, and landing (EDL) phase. However, Iris was modified to do these two functions. A simplified block diagram of the unit is shown Figure 3 along with the UHF receiver slice. To support the dual-band reception (one at UHF and one at X-band) without having to use two Analog-to-Digital Converters (ADC), a shared IF chain approach is taken [5]. The corresponding front-end RF

electronics for each band is switched on or off depending on the selected band. This reduces the volume need by eliminating a duplicate IF chain and ADC, but ultimately results in supporting only one band at one time. The radio is physically built by stacking together five modular slices as shown in Figure 1 (the middle).

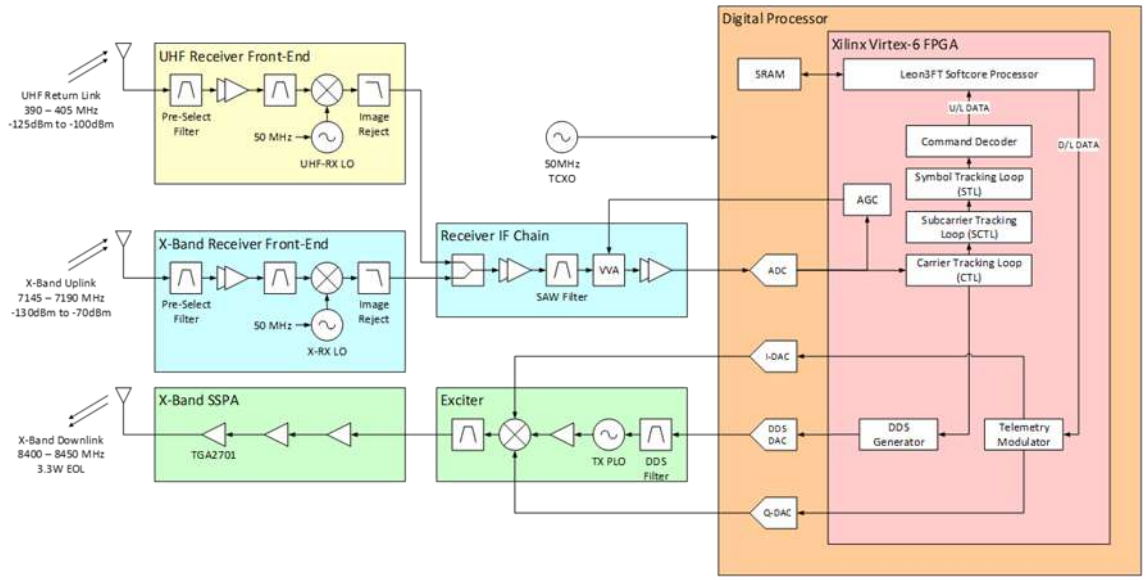

Fig. 3. Iris V2 (MarCO) Simplified Block Diagram

IRIS V2.1 (ARTEMIS-1 VERSION)

Iris V2.1 Upgrades and Improvements

Several upgrades were made to the Iris radio V1.0 for both MarCOs and the Artemis-1 CubeSat missions. The changes include a volume reductions of 30% between V2.0 and V2.1. The Virtex-6 defense-grade FPGA was chosen as an improvement from Iris V 1.0 which used a smaller Virtex-5 FPGA that lacked room for an embedded processor. An embedded softcore processor in the FPGA eliminates the need of a separate dedicated processor chip and reduces volume needs. The Virtex 6 FPGA was screened for heavy-ion induced Single-Event Latch-up (SEL) at the Texas A&M Cyclotron Institute and no SEL event was observed at a linear energy transfer (LET) of 37 MeV-cm2/mg [5]. Rad-hard memory devices are used for program memory (2 MB SRAM, EDAC protected) along with a rad-hard 32 MB NOR FLASH for storing bit stream configuration files and application software builds. The 32 MB of Flash memory provides non-volatile storage area for software images and the FPGA configuration file. Because there is no supervisory housekeeping FPGA to check for bit errors in the configuration file, the digital board instead takes advantage of the Xilinx FPGA's fallback configuration to allow booting from different bit stream files at power on. When the FPGA attempts to configure from a corrupt configuration file, it will autonomously reattempt configuration by falling back to another memory bank, improving the overall robustness of the radio. A third bit stream bank can be used to load in-flight bit stream updates to the radio without affecting the original configuration file as well. The fault-tolerant version of the LEON core includes advanced features to withstand and correct arbitrary single-event upset errors without loss of data, critical for reliable operation in deep-space environments. The fault-tolerance is provided at design level, and does not require a radiation-hardened semiconductor process, nor a custom cell library or special back-end tools. Another key improvement is the changes made to the power supply board. Previous versions of the power supply were mission-specific designs with lower ionizing dose requirements (e.g.: 2.9 krad for Mars trajectory), but with Artemis-1 missions baselining longer mission durations, some redesign was necessary to increase the radiation tolerance. Space-grade radiation-hardened switching converters are typically bulky hybrid devices that require large volume and mass. Instead, converters built on bipolar technology were chosen for their immunity against destructive latch-up from singular events caused by highly energetic particles [5]. For more detailed description of Iris V2.1 and tests and verification results, see [5].

Iris V2.1 Architecture

Iris is an SDR based on other JPL radio products like the Electra Proximity Radio [1] and the Universal Space Transponder [2]. The direct inheritance of previously-flown digital signal processing algorithms like tracking loop algorithms, forward-error correction coding schemes, error detection and correction (EDAC) modules, and the phase shift ey (PSK) modem allowed rapid development of the compact advanced-capability SDR. The Artemis-1 units are all configured for

operation in the X-band Space Research frequencies occupying 7.2 GHz uplink and 8.4 GHz downlink, but the modular radio architecture allows easy reconfiguration of the radio for other frequencies such as S- and Ka-band with interchangeable Radio Frequency (RF) front-end slices.
The uplink signal is first digitized by the Analog-to-Digital Converter (ADC) after down-conversion and amplitude leveling by the Voltage Variable Attenuator (VVA) in the front-end electronics. The tracking loops implemented on Iris are fully digital second-order phased-lock loops (PLL) with configurable loop bandwidth settings. The coherent turn-round approach takes the derived frequency from the uplink carrier signal and feeds this to a direct digital synthesizer (DDS) to tune the downlink phased-lock oscillator (PLO). This approach provides a simple method with fewer components that allows miniaturization while maintaining the necessary frequency agility from the transponder. The main oscillator is a 50 MHz Temperature Compensated Crystal Oscillator (TCXO). This reference signal is also used to generate the Local Oscillator (LO) frequency for block down-conversion in the receive chain.

The main interface to the spacecraft is via a Serial Peripheral Interface (SPI) bus at 1 MHz line rate. SPI commands from the flight on-board computer can configure the Iris software and various modem parameters, as well as transfer downlink data to Iris. SPI bus testing shows the interface can operate reliably up through 4 Mbps. At higher downlink data rates, this maximum SPI line rate and software processing times will limit the effective throughput. Hardware elements are in place to allow high-rate data interfacing via SpaceWire in the future [5].
The digital processing module houses an Analog-to-Digital Converter (ADC) to sample the uplink signal. The total power detector and automatic gain control (AGC) adjusts the signal level of the sampled signal to keep the input power to the ADC close to the optimal performance point to balance the needs of instantaneous dynamic range and binary resolution. The receiver tracking loops are full digital implementation, and the transmit carrier is Doppler tracked in coherent turn-around mode using a DDS. A pair of In-phase/Quadrature (IQ) Digital-to-Analog Converters (DAC) modulates the transmit waveform to the downlink carrier, allowing expansion capabilities to include any complex modulation and pulse shaping format within its bandwidth.

Iris V2.1 Firmware and Modem Signal Processing Description

The firmware architecture uses a minimal SPARC-based LEON system that consists of an embedded fault-tolerant processor, clock and reset generator, bus controllers, and memory controller (Figure 4). The architecture is centered on an Advanced Microcontroller Bus Architecture (AMBA) Advanced High-speed Bus (AHB), to which the LEON core and most high-bandwidth cores are connected. Other low-bandwidth units connect to the AMBA Advanced Peripheral Bus (APB), which is accessed through an AHB-to-APB bridge [5]. The fault-tolerant version of the LEON core includes advanced features to withstand and correct arbitrary single-event upset errors without loss of data, critical for reliable operation in deep-space environments.

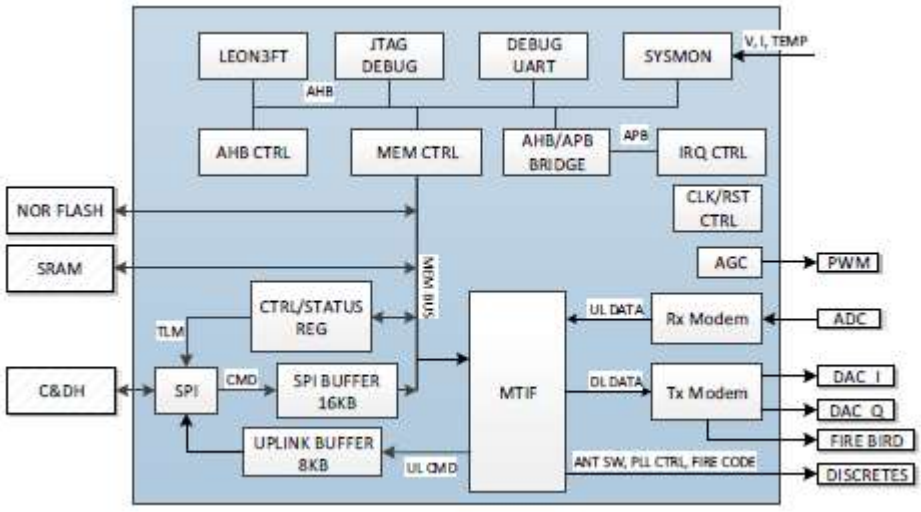

Fig. 4. Iris V2.1 Firmware Architecture Top-Level Block Diagram

Upon power-on of the radio, the FPGA configuration is auto-loaded, and the boot loader is executed. The boot loader decompresses the software application, configures various processor parameters, loads the application into the program area of memory, and sets the stack pointer to the start address location for application loading. The software then continues to configure and operate the radio.

Iris software on V2.0/V2.1 performs framing for downlink, where for Iris V1.0 the framing had to happen on the C&DH. Similar to Iris V1.0, Iris V2.0 & V 2.1 rely on the MTIF module to perform the data-handling functions for uplink and

Table 1. Iris Specifications and Comparisons Summary

Iris Specification	Units	Iris V1.0 INSPIRE Version	Iris V2.0 MarCO Version	Iris V2.1 Artemis-1 Version
Digital Processor		Xilinx Virtex-5 (commercial-grade)	Xilinx Virtex-6 (Industrial-grade)	Xilinx Virtex-6 (defense-grade)
Embedded CPU		N/A	SPARC-Based Leon3-FT Softcore	SPARC-Based Leon3-FT Softcore
No. Of Slices		4	5	4
Mass (excl. SSPA/LNA)	grams	450	1200	860
Volume (excl. SSPA/LNA)	U	0.46	0.77	0.56
Memory		32 Mbit NOR-Flash 128 Mbit Phase-Change Memory chip for the SPI interface	32 Mbit NOR-Flash 16 Mbit SRAM 4 Mbit EDAC SRAM	32 Mbit NOR-Flash 16 Mbit SRAM 4 Mbit EDAC SRAM
S/C Interface		1 MHz SPI±	1 MHz SPI	1 MHz SPI
Bus Power Interface	Vdc	6.4 - 8.4	10.5 – 12.3	9.0 – 28.0
DC Power	W	13.0	30.0 (including 5-W SSPA)	30.0 (including 5-W SSPA)
RF Output Power	W	0.5	5.0	5.0
Receiver Noise Figure	dB	5.0 – 6.0	3.5	3.5
Receiver Sensitivity	dBm	-135 @ 70 Hz LBW	-139 @ 70 Hz LBW	-151 @ 20 Hz LBW
Downlink Frequencies	MHz	8400 - 8500	8400 - 8500	8400 - 8500
Uplink Frequencies	MHz	7145 - 7235	7145 - 7235	7145 - 7235
Turn-around Ratio		880/749	880/749	880/749
Uplink Date Rates	bps	1,000	62.5 & 1,000	62.5 - 8,000
Downlink Data Rates	bps	62.5 - 64,000	62.5 & 1,000 & 8,000	62.5 - 256,000
UHF Receive Freq	MHz	N/A	390 - 405	N/A
UHF Rertun Link Rate	bps	N/A	8,000	N/A
Modulations Waveforms		PCM/PSK/PM w/ subcarrier PCM/PM w/ biphase-L, BPSK	PCM/PSK/PM w/ subcarrier PCM/PM w/ biphase-L, BPSK	PCM/PSK/PM w/ subcarrier PCM/PM w/ biphase-L, BPSK
Telemetry Encoding		Conv & Reed Solomon	Turbo 1/6	Conv & Reed Solomon Turbo ½, 1/3, 1/6
Navigational Support		Doppler, SR*	Doppler, SR, DDOR†	Doppler, SR, DDOR
Radiation Tolerance	krads	N/A	15.0 TID‡	23.0 TID

±SPI: Serial Peripheral Interface bus

* SR: Sequential Ranging

†DDOR: Delta Differential One-way Ranging

‡TID: Total Ionizing Dose

downlink. On Iris V2.1, decoded uplink commands are pushed into the uplinked buffer for collection by the C&DH and is primarily handled outside the context of the software for simplicity. Downlink data on the other hand includes software processing to form standardized frames prior to encoding in MTIF. The transmit portion of the modem contains mainly the telemetry modulator comprised of a subcarrier and direct-carrier modulator. In subcarrier mode, the transmit carrier generator is fed with the modulated subcarrier, the turnaround ranging tone, or the sum of both. In direct-carrier mode, the transmit carrier (no subcarrier) is complex multiplied with the telemetry data. Differential One-way Ranging (DOR) tones can be modulated on top of the telemetry modulation.

The receive portion of the modem is made up of the total power AGC, tracking loops, and demodulator modules. The carrier tracking loop acquires and tracks the carrier frequency and phase for Doppler compensation. After carrier and subcarrier acquisition, an early-late gate symbol synchronizer manages the timing of the integrate-and-dump filters to demodulate the complex IQ waveforms into symbols. Before the recovered symbols are passed to the uplink handler, single-bit error correction and double-bit error detection is performed on the encoded uplink code blocks.

Iris V2.1 Software Description

The Iris software is a single-threaded interrupt-based application using the SPARC V8 instruction set and runs at the native clock rate of 50 MHz. Iris supports several pre-defined modes: Receive-Only, Transmit-Only, Transmit/Receive, Ranging, and DOR. The software performs two primary routines: SPI command handling (commands from C&DH to Iris) and downlink data processing. Earlier mission-specific applications for MarCO included additional tasks such as running frequency-sweep algorithms for carrier acquisition, and store-and-forward bent-pipe transmissions.

Once firmware detects a valid SPI command, the firmware places the command into the command buffer and sends an interrupt to software. Software will process each command by parsing the opcode, size code, and data fields, and alerts the C&DH via the Interrupt discrete line if any errors or unexpected values occur. Most commands perform specific configuration changes, including antenna selections, data rate changes, and coding selections. Some SPI commands require immediate response to the C&DH (such as telemetry reporting, interrupt status, and uplink data handling) and the firmware directly handles the SPI response packet.

The Iris software is responsible for the handling of the downlink data between C&DH and Iris firmware. Software has the capability of forming Advanced Orbiting Systems (AOS) Transfer Frames complaint to the Consultative Committee for Space Data Systems (CCSDS) [5]. If no valid downlink data is available, pre-defined idle frames are transmitted to help maintain symbol synchronization at the receiving ground station. The C&DH can configure Iris to either enable or disable its onboard AOS framing. If framing is enabled, then Iris will expect downlink data to be sent across the SPI bus as CCSDS Space Packets, and software will push the data into its framing engine which generates AOS Transfer Frames. If framing is disabled, then Iris expects downlink data to be sent across the SPI as AOS Transfer Frames of pre-defined length, and software will queue the frames in memory until transmission through the modem.

CONCLUSION AND FUTURE PLANS

This paper provided a description of the evolution of the JPL Iris transponder and provided a summary of the key design aspects and specifications. See Table 1, above, for a summary of the specifications of the different Iris versions. Future development plans include over-the-air re-programmability (through C&DH) of the Iris software and firmware, advanced radiometric support with pseudo-noise Delta DOR [7] and regenerative ranging, incorporation of SpaceWire interface for high-rate data transfers to S/C C&DH unit, incorporation of advanced coding algorithms like Low Density Parity Check (LDPC), and development of dual-band versions at X- and Ka-band for radio-science applications and full two-way UHF as well S-band capabilities. The modular architecture of JPL radio product lines provide adaptability to mission requirements for various radio service needs in the future.

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